Date: 03/11/2997

To: USPTO

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Serial No.	09/826,117
Filing date	01/09/2001
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constructing a one-to-one correspondence of said N Walsh codes with said N Discrete Fourier transform (DFT) codes such ~~that sequency said N Fourier transform codes such~~ that sequency corresponds to frequency, even codes correspond to even codes, and odd codes correspond to odd codes,

~~there are N Discrete Fourier Transform (DFT) codes each with N complex chips,~~

arranging said DFT codes ~~are arranged~~ in increasing frequency, ~~and~~ wherein each code is the complex addition of a real axis code and an imaginary axis code,

constructing a mapping which uses said N Fourier codes to construct said DFT codes,

~~use~~ using said mapping and said correspondence of sequency and frequency, and even and odd codes to generate real and imaginary axis component codes of said hybrid Walsh codes,

said hybrid Walsh codes $\tilde{W}(c)$ with code index $c=0,1,2,\ldots,N-1$, are re-orderings of said Walsh codes defined by equations

for $c = 0$, $\tilde{W}(c) = W(0) + jW(0)$

for $c = 1,2,\ldots,N/2-1$, $\tilde{W}(c) = W(2c) + jW(2c-1)$

for $c = N/2$, $\tilde{W}(c) = W(N-1) + jW(N-1))$

for $c = N/2+1,\ldots,N-1$, $\tilde{W}(c) = W(2N-2c-1) + jW(2N-2c)$

wherein $W(u)$ is said Walsh code for index u and $j=\sqrt{-1}$,

~~digital signal processors in the transmitter encoder and receiver decoder for CDMA communications have a memory assigned to said Walsh codes and memories assigned to said real axis and imaginary axis codes of said hybrid Walsh codes,~~

generating hybrid Walsh codes ~~are generated~~ by reading code chip values from ~~said~~ Walsh code memory and writing to said hybrid Walsh code memory, ~~ies using addresses specified by said re-orderings of said Walsh codes,~~

reading said hybrid Walsh codes ~~are read~~ from said Hybrid Walsh

code memory and, ~~real and imaginary axis memories using said addressing for Walsh codes and,~~ using said hybrid Walsh codes ~~are implemented in the CDMA~~in a encoder for a CDMA communications link transmitter ~~said transmitter and in the CDMA decoder for said receiver~~ by replacing existing said Walsh real codes with said hybrid Walsh complex codes ~~using the same code vector indexing.~~ and in a decoder for said communications link receiver, in order to spread the data symbols over the transmission bandwidth.

Claim 8. (currently amended) The method of claim 7 wherein said codes have properties:

code chips take values {1+j, -1+j, -1-j, 1-j} in the complex plane,

code chips with a renormalization and rotation of the code matrix take values {1, j, -1, -j} in said complex plane,

inphase axis codes of said codes are re-ordered Walsh or Hadamard codes and,

quadrature axis codes of said codes are re-ordered Walsh or Hadamard codes.

Claim 9. (currently amended) The method of claim 7, further comprising the steps of: ~~A method for implementation of generalized hybrid Walsh codes for CDMA from code sets which include said hybrid Walsh, said Hadamard, said Walsh, said DFT, and pseudo noise (PN), said method comprising:~~

using tensor products also called Kronecker products ~~are used~~ to construct ~~said codes~~a second code which is a generalized hybrid Walsh code,

whrein an example 24 chip tensor product code is constructed from a 8 chip hybrid Walsh code and a 3 chip discrete Fourier transform DFT code,

said 24 chip tensor product code is defined by a 24 row by 24 column code matrix C_{24} wherein row vectors are code vectors and column elements are code chips,

said 8 chip hybrid Walsh code is defined by a 8 row by 8 column code matrix $\tilde{W}_8$,

said 3 chip DFT code is defined by a 3 row by 3 column code matrix E_3,

said C_{24} is constructed by tensor product of said $\tilde{W}_8$ with said E_3 defined by equation

$$C_{24} = \tilde{W}_8 \otimes E_3$$

wherein symbol "⊗" is a tensor product operation,

row u+1 and column n+1 matrix element $C_{24}(u+1,n+1)$ of said C_{24} is defined by equation

$$C_{24}(u+1,n+1) = \tilde{W}_8(u_0+1,n_0+1)\ E_3(u_1+1,n_1+1)$$

wherein

~~$u+1 = u_0u_1+1 + 3(u_1u_0+1)$~~

~~u~~ $= 0,1,\ldots,23$

~~$n+1 = n_0n_1+1 + 3(n_1n_0+1)$~~

~~n~~ $= 0,1,\ldots,23$

wherein u,n are code and chip indices for said codes C_{24} and u_0,n_0 are code and chip indices for said code $\tilde{W}_8$ and u_1,n_1 are code and chip indices for said code E_3,

~~digital signal processors in~~wherein said ~~transmitter~~ encoder and ~~receiver~~ said decoder for CDMA communications have memories assigned to ~~said~~ C_{24}, $\tilde{W}_8$, E_3 codes,

said C_{24} codes are generated by reading code chip values from said $\tilde{W}_8$ memory and said E_3 memory and combining using said equations to yield said chip values for said C_{24} and stored in said memory C_{24},

~~said chip values are combined using said equations to yield said chip values for said C_{24} codes and write to said C_{24} memory,~~

said C_{24} codes are read from said memory and implemented in said encoder ~~for said transmitter~~ and ~~in~~ said decoder ~~for said receiver~~,

~~an alternate method uses~~using direct products to construct ~~said~~a second code~~s~~ which is a generalized hybrid Walsh code~~.~~,

~~an~~ wherein an example 11 chip direct product code is constructed from said 8 chip hybrid Walsh code and said 3 chip DFT code,

said 11 chip code is defined by the 11 row by 11 column code matrix C_{11},

said C_{11} is constructed by direct product of said $\tilde{W}_8$ with said E_3 defined by equation

$$C_{11} = \tilde{W}_8 \oplus E_3$$

wherein symbol "$\oplus$" is a direct product operation,

row u+1 and column n+1 matrix element $C_{11}(u+1,m+1)$ of said C_{11} is defined by equation

$$\begin{aligned} C_{11}(u+1,n+1) &= \tilde{W}_8(u_0+1,n_0+1) \quad \text{for } u=u_0,\ n=n_0, \\ &= E_3(u_1+1,n_1+1) \quad \text{for } u=8+u_1,\ n=8+n_1, \\ &= 0 \qquad\qquad\qquad \text{otherwise,} \end{aligned}$$

~~said digital signal processors~~wherein ~~in~~ said ~~transmitter~~ encoder and said ~~receiver~~ decoder for CDMA communications have memories assigned to said C_{11}, $\tilde{W}_8$, E_3 codes,

said C_{11} codes are generated by reading code chip values from said $\tilde{W}_8$ memory and said E_3 memory and combined using said equations to yield said chip values for ~~said chip values are used by said equations to yield said chip values for~~ said C_{11} codes and ~~write to~~stored in said C_{11} ~~memory~~,

said C_{11} codes are read from memory and implemented in said encoder ~~for said transmitter~~ and ~~in said~~ decoder ~~for said receiver~~,

~~an alternate method uses~~using functional combining to construct ~~said codes~~a second code which is a generalized hybrid Walsh

code,

wherein an example 11 chip functional combined $\hat{C}_{11}$ code is constructed from said C_{11} codes by using codes to fill the two null subspaces of said C_{11}.

wherein said $\hat{C}_{11}$ codes are read from memory and implemented in ~~Said~~ said encoder ~~for said transmitter~~ and ~~in~~ said decoder ~~for said receiver and~~,

~~an alternate method uses~~using a combinations of tensor products, direct products, and functional combining to construct said generalized hybrid Walsh codes and,

~~which~~ said codes are read from memory and implemented in said encoder for ~~said transmitter~~a CDMA communications link and and ~~in~~ said decoder ~~for said receiver~~for said CDMA communications link.

Claim **10.** (cancelled)